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ABSTRACT

0034 A method and in-situ sample current amplification system for carrying out failure analysis of integrated circuit semiconductor device conductive portions. The method includes providing an integrated circuit (IC) semiconductor device; providing a pre-amplifier board (PAB) comprising current signal amplification electronics; mounting the IC semiconductor device in electrical communication with the PAB; mounting the PAB comprising the IC semiconductor device in a scanning electron microscope (SEM) for probing the IC semiconductor device with a primary electron beam; exposing at least a portion of the IC semiconductor device to the primary electron beam to induce a current signal within the conductive portions; amplifying the current signal; and, outputting the amplified current signal to an image display system to produce an image representative of an electrical resistance of the conductive portions.